

Figure 6-8. ADARIO data format.

6.15 <u>Submultiplex/Demultiplex Standards for Multiple Data Channels on a</u> <u>Primary Digital Multiplex/Demultiplex Channel</u>

For combining multiple low to medium rate telemetry channels on a single primary digital channel such as the ADARIO input channel, the submultiplex (submux) format is recommended. The format was developed for test range applications where high quantity of channels must be collected in conjunction with high data rate primary channels. The submux format provides a standard for extending the ADARIO primary channel or any other primary digital channel for conveying data from up to 31 subchannels in digital aggregate data form. Each channel is totally autonomous and can be enabled/disabled at any time. Some of the features of the submux format are

- accommodates analog, digital clocked and asynchronous, time and annotation text, and other application specific telemetry channels;
- requires less than 0.3 percent of overhead per channel;
- stores all necessary parameters for channel signal reconstruction in real or scaled time;
- preserves phase coherence between all channels for all rates (dc to maximum) and all types of channels; and
- accommodates variable and fixed rate primary channel of up to 256 Mbps.

6.15.1 Format Structure. General structure of the submux format is based on a constant block rate and variable block data length for each channel data block. The aggregate data stream is the sequential collection of each enabled channel data block with a three-word header. Each channel data block is the sequential collection of data samples or events within the block time period. A reserved channel (channel ID=31) provides frame synchronization and block timing and is always the first channel in the frame sequence. Individual channels can be enabled or disabled at any time within the rate limitations of the primary channel. Primary channel redundant parameter fields such as date, time, and annotation are placed in optional defined channel types, thereby, minimizing overhead caused by redundancy. All data and headers are bit packed into 16-bit words. All fields, unless specifically stated, are binary coded. Physical implementation of the format may have design restrictions as to types and quantities of channels and maximum allowable field limits.

6.15.2 <u>Implied Parameters and Limits</u>. Maximum aggregate rate (256 Mbps), block rate, first sample time delay measurement, and internal sample period are based on a 16-MHz clock rate divided by 2_N , where N can be set from 0 to 7 defining the derived clock. Block rate is based on the derived clock divided by 20 160 which sets the limit on the total aggregate word count of all channels in a block period. The maximum block rate (793.65 blocks per second) in conjunction with the 16-bit bit count field, limits the maximum subchannel input rate to 52 Mbps. The 16-MHz clock limits the time delay resolution to 62.5 nanoseconds.

The maximum number of channels is limited by the 5-bit field and the reserved block sync channel to 31 channels numbered from 0 to 30. Channel ID of 31 is the reserved block sync channel that conveys timing information. To accommodate fixed rate primary channel, fill can be inserted after the last channel data block, prior to the next block sync channel (at the end of the frame), and must consist of all binary ones (FFFF hex word value).

Channel priority is fixed in channel number sequence with channel ID of 31 (block sync) first, followed by channel ID 0, if enabled, to channel ID 30, followed by fill (if required) to maintain fixed channel rate. Any channel can be one of eight channel types. Type 0 channels convey timing data in the 3-word header and have implied data length of 0. Type other than zero contains the bit count field that defines the length of valid data in the data block. The actual word length of the data block is the integer of ((Bit Count + 15)/16). Channel type also defines the content of the fields in the header.

6.15.3 <u>Defined Parameters</u>. Each channel data block has a 3-word (16-bit) header that contains the channel ID number, channel type, and other defined and undefined fields based on the channel type code. Undefined fields are reserved for future use and should be zero filled. Each channel header also contains up to 4 status bits that indicate the condition in the current data block or the condition of the last aggregate frame.

Channel ID 31 is a special form of channel type 0. The first two words are used for synchronization and are F8C7 BF1E hex value. The block rate clock (BRC) defines the main clock binary divider and is used for time scaled signal reconstruction. Each increment time period doubles. "Fill" indicates if the primary channel requires fill for fixed data rate.

Channel ID can be any unique number from 0 to 30 and designates the physical subchannel used for acquiring the data. Channel type defines the type of data this channel conveys and is currently defined for 0 to 5.

A type 0 "Time Tag" channel typically processes IRIG time code data and is used to time tag the frame. The Days Hours Minutes Seconds Fractional Seconds fields are the content of IRIG time code input or channel derived and in the same BCD form as the IRIG G time code.

Type nonzero headers contain FMT field that defines the format of the sample in bits per sample, 4-bit status field that indicates any errors or warnings pertaining to the current data block, bit count field that defines the length of valid data in the data block, and time delay field that (when external clock is used) indicates the delay from block time to the first sample in the BRC defined clock periods. When the internal clock is used, as indicated by type or most significant bit (MSB) of time delay, the sample period field defines the period of the internal sample clock in the BRC defined clock periods. The internal sample clock is always an integer divisor of the block period and the first sample is coincident with the block time. In type 1 blocks, this field is used for sequential block count.

When the internal clock is used with digital serial channel, the data and clock lines are sampled at the designated rate and result in eight data and eight clock samples per data block word. Otherwise, all incoming digital data are sampled at the incoming clock and results in a sample in the data block, with the first sample being left justified in the first word with "format" designated number of bits starting with the MSB of the sample. Samples are bit sequentially packed regardless of word boundaries. The last sample in the block period is fully packed into the current data block with the remaining portion of the word, if any, being left undefined.

6.15.4 <u>Aggregate Format on the Primary Data Channel</u>. Figures 6-9a and b show the defined types of channel data from which the aggregate is composed. The primary data will always consist of the "Frame Sync" block followed by one or more unique channel blocks, followed by fill if required. The frame sync block will be generated at block rate. Aggregate data may be clocked by the primary channel or by the submux at constant or burst rate depending on the primary channel characteristics. Data format field definitions appear in appendix G, Submux Data Format Field Definitions.

6.15.5 <u>Submux/Demux FILL Requirement</u>. The submux produces aggregate data at the user aggregate data rate. In other words, the rate and amount of data produced on the aggregate output is directly proportional to the user specified clock and data format bits and is averaged over the frame period. This variable aggregate data rate is acceptable to variable rate primary channels or buffered variable rate recorders.

Fixed rate primary channels and fixed rate recorders require data at some fixed rate. The fixed rate is usually set to be the maximum expected user aggregate rate. When the user aggregate rate is less than the maximum, then some sort of filler is necessary to maintain the constant output rate. The format-specified fill word provides this filler and is automatically generated when the primary channel or fixed rate recorder provides clocks after the last word of the last enabled channel is clocked out within the frame period. Fill is always terminated by the Frame of Block Sync channel, indicating the presence of the next frame data.

The quantity of fill words is totally dependent on the fixed primary channel rate and the average user aggregate rate within one frame period. Minimum is zero words when user rates are at the maximum and equal to the fixed rate (minus the overhead). When user rates are at the minimum, maximum amount of fill will be generated for maintaining constant output rate.

									16	BITS							
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GENERAL FORM	HW1			CHN II	D			CHT			F	FMT		ST1	ST2	ST3	ST4
	HW2 HW3	I/E						TIME	E DELAY	(OR SA	MPLE I	PERIOD)				
FRAME SYNC	HW1		C	'HN ID -	- 1F			CHT – ()			SYNC 1	- F8C7 F	IFX (FU		<u>(</u> D)	
I IO INLE DI INC	HW2		U		- 11			<u>S</u>	, YNC 2 =	BF1E H	IEX	<u>bine i</u>	-100/1			(D)	
	HW3		BRC		FILL									AOE	PCR	ST3	ST4
		<u></u>															
TIME TAG	HW1		CHN	ID = 0	TO 30			CHT = ()			Ν	ASB I	DAYS (E	BCD)		
	HW2	DA	AYS			HOUF	RS (BCD))					MIN	UTES (I	BCD)		
	HW3	SECONDS (BCI					D)						FRACTI	ONAL S	ECOND	S	
ANNOTATION	HW1		CHN	ID = 0	TO 30			CHT =			FN	/IT = 7		NC	OVR	PE	OE
TEXT	HW2								BIT C	COUNT	_						
	HW3	MGD	1.0						BLOCK	COUN	T	O GU A D	A CITED				
	DWI	MSB	15	ГСНАК	RACIER					MSB	21	J CHAR	ACTER				
	DWN	MSB	LA	ST CH	ARACTE	R						UN	DEFINED	IF NO	LAST		
	Dirit	MDD	L		IIIIEIE	IX.				I		010		I 110	1 12/10/1		
DIGITAL SRL	HW1		CHN	J ID = 0	TO 30			CHT = 2	,		FM	$\mathbf{T} = 0$		NSIB	OVR	ST3	ST4
EXT. CLK	HW2		CIII	$(\mathbf{ID} = 0)$	10.50			0111 - 2	BIT CC	UNT =	L	11 - 0		TIGID	0,14	515	511
	HW3	I/E=0							TI	ME DE	LAY						
	DW1	DS ₁	DS ₂	DS ₃	DS_4	DS ₅	DS ₆	DS ₇	DS ₈	DS ₉	DS ₁₀	DS_1	DS_{12}	DS ₁₃	DS ₁₄	DS ₁₅	DS ₁
	:			1		1			1								
	DWN							DS _{L-1}	DSI			UN	DEFINED	IF NO	Γ LAST		

Figure 6-9a. Submux data format.

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[15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DICITAL ODI	LIW /1		CUN	ID = 0	FO 20			CUT - 2	1		EM	IT – 0		0	0	ST2	ST4
	INT CLK	HW1 HW2		CHN	ID = 0	10.50			CHI = 2	BIT CO	$\begin{array}{c c c c c c c c c c c c c c c c c c c $					514		
	IIVI. CLIX	HW2 HW3	I/E=1								0111 - 1		SAN	IPLE PE	RIOD			
		DW1	DS ₁	DS ₂	DS ₃	DS_4	DS ₅	DS ₆	DS ₇	DS ₈	CS_1	CS ₂	CS ₃	CS_{4}	CS ₅	CS ₆	CS_7	CS ₈
		:					5	0	,	0			5		5	Ŭ	,	Ŭ
		DWN	DS _{L-}	DS _{L-}	DS _{L-}	DS _{L-}	DS _{L-}	DS _{L-}	DS _{L-}	DSL	cs _{L-}	cs _{L-}	cs _{L-}	cs _{L-}	cs _{L-}	CS _{L-}	cs _{L-}	CSL
		-																
	DIGITAL PRL.	HW1		CHN	ID = 0	ГО 30			CHT = 3		FMT	=0 TO 1	5 (SHOW	VN =6)	NSIB	OVR	ST3	ST4
	EXT. CLK	HW2		1						BIT CO	UNT = I							
		HW3	I/E=0	TIME	DELAY					MGD		A 11D						
		DW1	MSB		ISTS	AMPLE				MSB		2ND	SAMPLE	<u>i</u>			3RD SA	MPLE
<u>6</u>		DWN		MSB LAST SAMPLE I SB-BIT I UNDEFINED IE NOT LAST														
39		2		1102	21101	5111112		<u></u> 511	-		01122			21101				
	ANALOG	HW1	CHN II	D = 0 TC) 30			CHT =	4		FMT=0) TO 15	(SHOW)	N =7)	AOR	ST2	ST3	ST4
	WIDE BAND	HW2				-				BIT CO	UNT = I	4					•	
		HW3	I/E=1									SAMPL	E PERIO	D				
		DW1	MSB		1ST SA	MPLE					MSB		2^{NE}	SAMPL	Æ			
		:																
		DWN	MSB		LAST S	SAMPLE							UND	EFINED	IF NOT	LAST		
			_															
	ANALOG	HW1		CHN	ID = 0	ГО 30			CHT = 5		FMT	=0 TO 1	5 (SHOW	VN =7)	LAO	RAO	ST3	ST4
	STEREO "I " & "D"	HW2	I/E-1	BIT COUNT = L														
	Lak	DW1	MSB	LINL	1ST SA	MPLE "I					MSB	SAMFL	L FERIO	SAMPLE	E "R"			
		:	MDD		101 0/1		_				MDD		151					
		DWN	MSB		LAST	SAMPL	E						UND	EFINED	IF NOT	LAST		
		-																
	FILL	FW							FILI	L WORD	= FFFF	HEX						

Figure 6-9b. Submux data format.

6.16 <u>1/2 Inch Digital Cassette (S-VHS) Helical Scan Recording Standards</u>

These standards are for helical scan digital magnetic tape recorder/reproducers using the Very Large Data Store (VLDS) format. This standard is intended for applications where compact size is needed and bit rates do not exceed 32 or 64 megabits per second (Mbps). The VLDS is a 12.65 mm (1/2 inch) S-VHS (850 oersteds nominal) media based tape format. This standard describes the salient features of the LDS format. To ensure crossplay compatibility between recorders of different manufacturers, refer to Metrum Document Number 16829019¹.

6.16.1 <u>Tape and Tape Cartridge</u>. The tape shall conform to Magnetic Media Laboratory (MML) Document Number 93-1, <u>Specification for Rotary Instrumentation</u> <u>Magnetic Recording Tape, 68KA-M (850 oersteds</u>), dated 16 February 1993 and the tape cartridge shall conform to ANSI Standard V98.33M-1983, <u>Specification for</u> <u>Physical Characteristics and Dimensions</u>.

6.16.2 <u>Format Types</u>. There are four standard formats: two B formats provide 32 Mbps standard density or 64 Mbps high density for most applications where severe environmental conditions are not encountered, and two E formats provide 16 Mbps standard density or 32 Mbps high density for harsh environments involving extremes of vibration and temperature. A tape made on a standard density system may be reproduced on a high density system. Relative to the B formats, the E formats use a 100 percent larger track pitch, an 81 percent larger track width, and a larger guard band providing a very large margin for accurately tracking and recovering data under extreme conditions. The E formats provide only about one-half the data storage capacity of the B format but can be played back on a B format system.

6.16.2.1 <u>B Format</u>. These formats originate from helical scanner implementations using four helical heads organized in pairs at 180° separation. The heads are both read and write functionally and are supported by two parallel sets of read/write electronics referred to as data channels. Helical track dimensions are given in figure 6-10.

6.16.2.2 <u>E Format.</u> These formats originate from helical scanner implementations using two helical heads with wider track widths at 180° separation on the scanner. The heads are both read and write functionally. One set of read/write or write only electronics is required. Helical track dimensions are given in figure 6-11.

¹ Metrum Document Number 16829019, <u>VLDS Magnetic Tape Recorder/Reproducer</u> <u>Tape Cartridge Format Specification</u>. Available from Metrum, Inc., 4800 E. Dry Creek Road, Littleton, Colorado 80122.



Figure 6-10. Helical track dimensions, B format.



Figure 6-11. Helical track dimensions, E format.

6.16.3 <u>Data Storage</u>. Data are recorded onto 12.65 mm (1/2 in.) wide magnetic tape using both rotating and fixed heads (see figure 6-12). The rotating heads record data in adjacent track patterns at an inclined angle to the normal tape motion. The fixed heads record data on tracks parallel to the tape motion. The fixed head tracks are used for control and servo purposes and do not directly record user data.

6.16.4 <u>Physical Relationships</u>. Maintaining high accuracy of the ratio between scanner rotational speed and tape speed (1.5492 mm (0.0610 in.) of tape motion per scanner rotation) is critical to maintaining the format geometry. Head and tape speed will vary accordingly with changes in the other two speed parameters. The three speed parameters vary linearly with

desired user data rates. Parameters used with a user data rate of 32 Mbps (B) or 16 Mbps (E) are as follows:

user bits/helical track	2^{17} =131 072 bits (16 KBytes)
scanner diameter	62.000 mm + 0.008/-0.000mm
	(2.44 in. + 0.0003 in.)
scanner rotation speed	3662.1 rpm
tape speed	94.55 mm/sec (3.72 in./sec.)
head/tape speed	11 794.30 mm/sec (464.34 in./sec.)
helix angle (head rotational	5° 56' 7.4" basic dimension
plane to ref. edge of tape)	
head gap length	refer to Metrum Document 16829019
tape tension (inlet side of	0.35N <u>+</u> 0.02N
scanner)	

6.16.5 <u>Helical Track Organization</u>. Each group of four helical tracks resulting from one complete revolution of the scanner (two helical tracks for the E formats) is termed a principal block on the tape. A principal block is the smallest increment of data that may be written to or read from the tape. Each principal block is assigned a unique number which is recorded as part of the helical track. Helical tracks containing user data begin with the number 1 and are sequentially incremented on the tape up to the capacity of the cartridge. Whenever new data are appended on a previously recorded cartridge, the new data are precisely located to begin with the next helical track location after the previous end of data point with no interruption or discontinuity in track spacing.

6.16.6 <u>Recorded Information</u>. The following subparagraphs contain additional information.

6.16.6.1 Add overhead bytes generated by error correction encoding algorithms.

6.16.6.2 Provide preamble and postamble patterns for isolation of the information at the beginning and ends of the helical tracks.

6.16.6.3 Provide clock synchronization patterns to facilitate clock recovery at the beginning of each helical track.

6.16.6.4 Add patterns throughout the helical track to maintain synchronization and counteract bit slips during data extraction.

6.16.6.5 Provide redundantly recorded principal block numbers for organizing data on the cartridge.

6.16.6.6 Include a user specifiable volume label for identifying the entire cartridge.

6.16.6.7 Add miscellaneous data used to convey information about the organization of data on the cartridge and within the helical tracks.

6.16.7 <u>Recording Geometry and Physical Dimensions</u>. Included in the following subparagraph are the recording geometry and the physical dimensions.

6.16.7.1 <u>Tape Reference Edge</u>. The tape reference edge for dimensions specified in this section shall be the lower edge as shown in 6-12. The magnetic coating, with the direction of tape travel as shown in figure 6-10, shall be the side facing the observer.

6.16.7.2 <u>Helical Tracks</u>. Contained in the succeeding subparagraphs are the helical tracks attributes.

6.16.7.2.1 <u>Track Widths</u>. The width of a written track shall be $0.032 \text{ mm} \pm 0.002$ (0.0013 in. ± 0.000079) for the B formats and 0.058 mm ± 0.002 (0.0023 in. ± 0.000079) for the E formats.

6.16.7.2.2 <u>Track Pitch</u>. The distance between the center lines of any two adjacent tracks, measured perpendicular to the track length, shall be 0.0404 mm (0.0016 in.) for the B formats and 0.0808 mm (0.0032 in.) for the E formats.

6.16.7.2.3 <u>Track Straightness</u>. Either edge of the recorded track shall be contained within two parallel straight lines 0.005 mm (0.0002 in.) apart. The center lines of any four consecutive tracks shall be contained within the pattern of four tolerance zones. Each tolerance zone is defined by two parallel lines which are inclined at an angle of 5° 58' 58.4" basic with respect to the tape edge. The center lines of the tolerance zones shall be spaced 0.0404 mm (0.0016 in.) apart for the B format and 0.0808 mm (0.0032) apart for the E format. The width of the first tolerance zone shall be 0.007 mm (0.00028 in.). The width of tolerance zones two, three, and four shall be 0.011 mm (0.0004 in.). These tolerance zones are established to contain track angle, straightness, and pitch errors.

6.16.7.2.4 <u>Gap Azimuths</u>. The azimuth of the head gaps used for the helical track recording shall be inclined at angles of $\pm 6^{\circ} \pm 15'$ to the perpendicular to the helical track record (see figures 6-10 and 6-11). For the E formats and for the first and third tracks of every principal block of the B formats, the recorded azimuth is oriented in the clockwise direction with respect to the line perpendicular to the track direction when viewed from the magnetic coating side of the tape. For the B formats, the second and fourth tracks of each principal block are oriented in the counterclockwise direction.

6.16.7.2.5 <u>Track Guard Bands</u>. The nominal unrecorded guard band between any two adjacent helical tracks shall be 0.008368 mm (0.0003 in.) for the B formats and 0.022737 mm (0.0009 in.) for the E formats.

6.16.7.2.6 <u>Track Angle</u>. The track angle shall be 5° 58' 58.4".

6.16.7.2.7 <u>Track Length</u>. The track length shall be 96.619 mm (3.80 in.).

6.16.7.2.8 <u>Physical Recording Density.</u> The maximum physical density of the recording shall be 1930 or 3776 flux transistors per millimeter (ftpmm) respectively for the 32 and 64 Mbps systems.

6.16.7.3 <u>Longitudinal Tracks</u>. The characteristics of the longitudinal tracks are described in the subsequent subparagraphs.

6.16.7.3.1 <u>Servo Track</u>. The servo track is located along the reference edge of the tape as shown in figure 6-12. The azimuth angle of the servo track head gap shall be perpendicular to the recorded track. The recording of the servo track is composed of a recorded pulse (nominally 0.0185 mm (0.0007 in.)) for each principal block on the tape. The recording shall achieve full magnetic saturation for at least half the pulse. The time duration of the pulse is determined by the tape speed to yield this physical dimension. During the interval between pulses, no magnetic recording occurs on the track. The pulse is timed to begin coincident with the midpoint of the principal block (the data channel switches from first to second head). The physical offset from the longitudinal head to the helical heads is shown in figures 6-10, 6-11, and 6-12 as dimension "X."

6.16.7.3.2. <u>Filemark Track</u>. The filemark track is located near the top of the tape as shown in figure 6-12. The azimuth angle of the filemark track head gap shall be perpendicular to the recorded track. The recording of the filemark track is composed of a series of pulses located in conjunction with the principal block to be marked. Each filemark is composed of three redundant pulses (nominal 0.005 mm (0.0002 in.)). The three pulses are typically spaced 0.029 mm (0.0011 in.) apart with a maximum span of 0.09 mm (0.0035 in.) from the beginning of the first to the beginning of the third. This triplet of pulses is for redundancy against tape flaws and on detection are treated as one filemark regardless of whether 1, 2, or 3 pulses are detected. The filemark pulses are associated with a specific principal block by initiating the first pulse between 4 to 5.5 msec after the midpoint of the principal block. (Data channel switches from first to second head.)



Figure 6-12. Recorded tracks on tape, B format.

6.16.8 <u>Tape Cartridge Format</u>. The physical format of the recording along the length of the tape is shown in figure 6-13. Immediately following the physical beginning of tape (PBOT) is an unused portion of tape, followed by the cassette format zone which precedes the logical beginning of tape (LBOT). Principal blocks of user data shall be recorded between LBOT and the logical end of tape (LEOT), which precedes the physical end of tape (PEOT).



Figure 6-13. Tape cartridge layout.

6.16.8.1 <u>Load Point</u>. The load point is defined as the first point after PBOT accessible by the recording system with the tape fully engaged to the scanner.

6.16.8.2 Format Zone. The format zone begins at the load point, precedes the LBOT, and consists of a minimum of 450 principal blocks recorded on the tape. It provides a run up area for the servo systems and principal block identification allowing precise location of the LBOT where user data begin. The zone must be prerecorded to prepare the cartridge to accept user data. This process involves locating at the load point and beginning recording as soon as tape speed servo lock is achieved. The principal blocks recorded are numbered beginning with a negative number and counting up until principal block 0 is recorded. Principal block 0 shall be the last recorded block in the format zone. Principal blocks recorded in the format zone do not contain user data or error correction coding (ECC) overhead bytes, but do contain the remaining miscellaneous information described in paragraph 6.16.6 and in the helical track data format descriptions. The volume label for the cartridge is irreversibly determined at the time the format zone is recorded.

6.16.8.3 <u>Logical Beginning of Tape</u>. The logical beginning of tape denotes the end of the format zone and the point at which principal blocks containing reproducible data begin. The first principal block containing useful information shall be assigned the number one.

6.16.8.4 <u>Data Zone</u>. Beginning with principal block 1 at LBOT and continuing through to LEOT, the data zone shall be the principal blocks which record user data as well as the added miscellaneous information to allow full reproduction and management of the data on the tape cartridge.

6.16.8.5 <u>Logical End of Tape</u>. The logical end of tape is a physical principal block count. The principal block count for the standard ST-160 tape cartridge is 210 333.

6.16.9 <u>Helical Track Format</u>. The format for writing data into a single helical track is shown in figure 6-14. The term "bits" refers to actual on tape bit cells. Each helical track begins with a preamble area consisting of 6216 bits of an alternating pattern of three 0 bits and three 1 bits for the 32 Mbps system or 9240 bits for the 64 Mbps system. This 6-bit pattern is repeated 1036 or 1540 times. The preamble is followed by a track synchronization area. This area provides for obtaining registration to the track data patterns. It is composed of four zones of 732 bits each with an alternating 0 and 1-bit pattern that facilitates clock recovery. Each of these four zones is followed by a 36-bit sync pattern. These sync patterns are described more fully in subparagraph 6.16.9.1. The track synchronization area ends with 24 bits of an alternating pattern of three 0 bits and three 1 bits. The central area is where actual user data are recorded in 138 data blocks for the 32 Mbps system or 276 data blocks for the 64 Mbps system. Each data block contains 205 5/6 modulation code frames of interleave data for a total of 1230 bits.



Figure 6-14. Helical Track Format.

This data is followed by a 36-bit sync pattern. Sync patterns and interleave data are more fully described next. Each helical track ends with a postamble pattern of three 0 bits and three 1 bits. This is the same pattern as the preamble. Compiling all bits yields an overall track total of 186 468 tape bits for the 32 Mbps system and 364 824 tape bits for the 64 Mbps system. Since each contains 131 072 or 262 144 user bits, overheads are 29.7 and 28.1 percent.

6.16.9.1 <u>Sync Patterns</u>. Each helical track contains 142 or 280 sync patterns as shown in figure 6-14. Four of these are contained in the track sync area with the remaining 138 or 276 distributed at the end of each data block. These sync patterns provide registration to the bit sequence and allow management of bit slips. The track and data sync consists of 36 bits in the form of six 6-bit words. The first five words are the same for all sync words. They are

WORD0	2A _h	WORD3	0F _h
WORD1	2A _h	WORD4	$2l_h$
WORD2	0C _h		

WORD5 defines which sync word is being issued in the following manner:

Sync Location	Words	Sync Location	Words
Track Sync 1	39 _h	Data Sync 4	2E _h
Track Sync 2	35 _h	Data Sync 5	2B _h
Track Sync 3	2D _h	Data Sync 6	2E _h
Track Sync 4	1D _h		
Data Sync 1	2B _h		
Data Sync 2	2E _h	Data Sync 279	2B _h
Data Sync 3	2B _h	Data Sync 280	2E _h

6.16.9.2 <u>Data Blocks</u>. Each helical track contains 138 or 276 data blocks which record the user data as well as miscellaneous information used in locating and managing data on the tape cartridge (see figure 6-14). The construction of these data blocks is performed by each channel's data path electronics. Figure 6-15 illustrates a typical block diagram of a channel data path as described in the following subparagraphs.

6.16.9.2.1 <u>Error Correction Encoding</u>. An interleaved Reed-Solomon (RS) code is used for error detection and correction. An outer ECC is applied to written data first which is an RS (130, 128) for purposes of error detection only. An inner ECC is subsequently applied which is an RS (69, 65) for error detection and correction. The resulting encoded data is stored in a multiple page interleave buffer memory array containing 128 rows by (2x69) or (8x69) columns of encoded user data. For the outer ECC, incoming data is arranged in groups of 128 bytes each. The outer ECC encoder appends 2 check bytes to each 128 byte block. For the inner ECC, the 130 byte group resulting from the outer ECC is divided into two 65 byte blocks. The first 65 byte block (ECC codewords 1, 3, 5, ...) contains all user data while the second 65 byte block (ECC codewords 2, 4, 6, ...) contains 63 bytes of user data with the last 2 bytes being the check bytes generated by the outer ECC. The inner ECC encoder appends 4 check bytes to each 65 byte block.



Figure 6-15. Typical VLDS data path electronics block diagram.

Operations in the RS encoder are performed using numbers in a finite field (also called a Galois field (GF)). The field used contains 256 8-bit elements and is denoted GF (256). The representation of GF (256) used is generated by the binary degree eight primitive polynomials.

$p(x) = x^{\delta}$	8 +	x^4	+	x ³	+	\mathbf{x}^2	+	1	outer ECC
$p(x) = x^{\delta}$	8 +	x^5	+	x^3	+	х	+	1	inner ECC

The ECC generator polynomials are

$$G(x) = (x+a^{24}) (x+a^{25}) \qquad \text{outer ECC} \\ G(x) = (x+1) (x+a) (x+a^2) (x+a^3) \qquad \text{inner ECC}$$

where "a" denotes the primitive element of the field.

6.16.9.2.2 <u>Interleave Buffer</u>. Encoding data from the two levels of ECC are stored in an interleave buffer memory. The architectures for this memory are shown in figure 6-16. This buffer allows interleaving of the encoder data. Interleaving spreads adjacent ECC code word bytes within a helical track for the 32 Mbps system to minimize the effect of burst error events. For the 64 Mbps system, interleaving spreads adjacent ECC codeword bytes within two helical tracks (two helical tracks per channel per principal block) to further minimize burst error effects. Data to and from the ECC are accessed along horizontal rows in the memory matrix. Data to and from tape are accessed along vertical columns in the memory. Each column in the matrix consists of 128 bytes which will constitute one block in the helical track format (see figure 6-14).

6.16.9.2.2.1. <u>Exchange of Data with ECC</u>. Addressing of the interleave buffer for exchange of data with the ECC for the 32 Mbps systems is

ECC CODEWORD	ADDRESS RANGE (hexadecimal)
1	0.080 to 0.0074
1	0000 to 0024
2	
3	0180 to 01C4
4	0100 to 0144
5	0380 to 03C4
ECC CODEWORD	ADDRESS RANGE (hexadecimal)
6	0200 to 0244
•	•
253	7E80 to 7EC4
254	7E00 to 7E44
255	7F80 to 7FC4
256	7F00 to 7F44



Figure 6-16. Interleave buffer architectures.

Addressing of the interleave buffer for exchange of data with the ECC for the 64 Mbps systems is

ECC CODEWORD	ADDRESS RANGE (hexadecimal)
1	00000 to 00044
1	
2	00400 to 00444
3	00800 to 00844
	·
128	1FC00 to 1FC44
129	00080 to 000C4
130	00480 to 004C4
•	·
•	·
256	1EC90 to 1ECC4
230	IFC80101FCC4
257	00100 to 00144
258	00500 to 00544
512	1FD80 to 1FDC4
513	00200 to 00244
514	00600 to 00644
011	
·	·
1024	$1EE90 \pm 0.1EEC4$
1024	17700 10 17704

Each codeword is 69 bytes long. The address increments by hex 001 for each byte in a codeword. The first data byte sent to/from the ECC for each helical track is stored in location 000.

6.16.9.2.2.2 <u>Exchange of Data To and From Tape</u>. Addressing of the interleave buffer for exchange of data to and from tape for the 32 Mbps system is

DATA BLOCK	ADDRESS RANGE (Channel 1)	ADDRESS RANGE (Channel 2)
1	0000 to 7F00	0022 to 7F22
2	0080 to 7F80	00A2 to 7FA2
3	0001 to 7F01	0023 to 7F23
4	0081 to 7F81	00A3 to 7FA3
5	0002 to 7F02	0024 to 7F24
6	0082 to 7F82	00A4 to 7FA4

•	•	•
•		•
•		•
67	0021 to 7F21	0043 to 7F43
68	00A1 to 7FA1	00C3 to 7FC3
69	0022 to 7F22	0044 to 7F44
70	00A2 to 7FA2	00C4 to 7FC4
71	0023 to 7F23	0000 to 7F00
•		•
	•	
135	0043 to 7F43	0020 to 7F20
136	00C3 to 7FC3	00A0 to 7FA0
137	0044 to 7F44	0021 to 7F21
138	00C4 to 7FC4	00A1 to 7FA1

DATA BLOCK ADDRESS RANGE (Channel 1) ADDRESS RANGE (Channel 2)

Addressing of the interleave buffer for exchange of data to/from the 64 Mbps system is

DATA BLOCK	ADDRESS RANGE (hexadecimal)
1	00000 to 1FC00
2	00080 to 1FC80
3	00100 to 1FD00
4	00180 to 1FD80
8	00380 to 1FF80
9	00001 to 1FC01
10	00081 to 1FC81
275	00122 to 1FD22
276	001A2 to 1FDA2
1'	00222 to 1FE22
2'	002A2 to 1FEA2
	00322 to 1FF22
• •	
 8'	001A3 to 1FDA3
0, 0,	00223 to 1FE23
1	00223 to 11 1223

Each data block is 128 bytes long. The address increments by hex 0100 for each byte in a data block. The first byte sent to/from tape for each channel 1 helical track is stored in location 0000. The first byte sent to/from tape for each channel 2 helical track is stored in location 0022.

DATA BLOCK	ADDRESS RANGE (hexadecimal)
10'	002A3 to 1FEA3
•	
•	•
275'	00344 to 1FF44
276'	003A4 to 1FFA4

Each data block is 128 bytes long. The address increments by hex 0400 for each byte in a data block. The first byte sent to or from tape for both channels is stored in location 00000. The interleave buffer extends across both helical tracks in a principal block for each channel, thus the data block number "n" refers to the data block in the first helical track of the principal block and the data block number "n" denotes the data block number in the second helical track of the principal block.

6.16.9.2.3 <u>8 to 5 Conversion</u>. Data being moved from the interleave buffer to tape is read from the memory in 8-bit bytes and is immediately converted to 5-bit groups in preparation for modulation coding. During reproduction this conversion occurs in reverse fashion. The algorithm for conversion is detailed in Metrum Document Number 16829019.

6.16.9.2.4 <u>Miscellaneous Information Inclusion</u>. Each data block in the helical track includes one additional bit added to the data set prior to modulation coding. Each data block removed from the interleaved buffer memory consists of 128 bytes of ECC encoded user data totaling 1024 bits. Conversion from 8-bit bytes to 5 bit groups results in 204 groups plus 4 bits. A miscellaneous information bit is added to each data block as the 1025th bit to complete 205 full 5-bit groups. Miscellaneous information is currently defined only in the first helical track of each principal block. The remaining three helical tracks (1 in the E format) contain no defined miscellaneous bits and are reserved for future expansion. Any reserved miscellaneous information bits shall be recorded as 0 bits. The defined purposes of miscellaneous information bits in the first helical track of each principal block are

DATA BLOCK 1 to 20 inclusive	MISCELLANEOUS BIT DEFINITION First copy of 20-bit principal block number: 2s complement binary; least significant bit in data block 1; most significant bit in data block 20.
21 to 40 inclusive	Second copy of 20-bit principal block number: 2s complement binary; least significant bit in data block 21; most significant bit in data block 40.

<u>DATA BLOCK</u> 41 to 60 inclusive	MISCELLANEOUS BIT DEFINITION Third copy of 20-bit principal block number: 2s complement binary; least significant bit in data block 41; most significant bit in data block 60.				
61 to 76 inclusive	Volume label: 16-bit binary; least significant bit in data block 61; most significant bit in data block 76.				
77 to 80 inclusive	Revision number: 4-bit code; value at time of writing is 0001 (1_h) .				
81 to 84 inclusive	 4-bit tape information code as follows: 81 bit = 0 denotes all helical data was input as user digital data. 81 bit = 1 denotes input data stream to each channel. The ECC was 15 bytes of user digital data beginning with first byte plus 1 inserted byte from a different source in a repeating fashion. This bit must be uniformly set for the entire cartridge including the format zone. It is used to support mixing of digitized analog data into the digital stream and separation on reproduction. 				
	82 bit = 0 denotes cartridge size is ST-120 for purposes of determining LEOT. This bit must be set for the entire cartridge including the format zone.				
	82 bit = 1 denotes cartridge size is ST-160 for purposes of determining LEOT. This bit must be set uniformly for the entire cartridge including the format zone.				

DATA BLOCK	MISCELLANEOUS BIT DEFINITION			
	83 and 84 Reserved for additional			
	tape information coding.			
85 to 138 or 276 inclusive	Reserved for future expansion			

6.16.9.2.5 <u>Modulation Code</u>. Data is encoded using a 5/6 modulation code that has a spectral null at dc. The coding algorithm employed has a code word digital sum (CWDS) maximum of \pm 2 with a maximum run length of 6 bits. The 205 5-bit groups resulting from the 8 to 5 conversion (including the inserted miscellaneous bit) undergo this coding to form the final 5/6 code frames that are physically recorded in the data blocks of the helical track format. The algorithm for coding is detailed in Metrum Document Number 16829019.

6.17 <u>Multiplex/Demultiplex (MUX/DEMUX) Standards for Multiple Data</u> <u>Channel Recording on ½ Inch Digital Cassette (S-VHS) Helical Scan</u> <u>Recorder/Reproducer Systems.</u>

For recording and reproducing multiple channels on 1/2 Inch Digital Cassette (S-VHS) Helical Scan Recorders, the Asynchronous Real-time Multiplexer and Output Reconstructor (ARMOR) multiplex/demultiplex format is recommended. The ARMOR data format is an encoding scheme that may be used to multiplex multiple asynchronous telemetry data channels into a single composite channel for digital recording, transmission, and subsequent demultiplexing into the original constituent channels.

6.17.1 <u>General.</u> Data types supported by the ARMOR format are PCM, analog, decoded IRIG time, and 8-bit parallel. MIL-STD-1553 data is encoded into an IRIG 106 Chapter 8 serial PCM stream prior to multiplexing into the ARMOR format. Voice channels are encoded in the same way as all other analog channels. The composite channel is formatted into fixed bit-length, variable word-length frames. A constant aggregate bit rate and a fixed frame bit-length are established for each multiplex by an algorithm that is dependent on the number, type, and rate of the input channels. The aggregate bit rate and frame bit length result in a fixed frame rate for each multiplex. The ARMOR encoding scheme captures the phase of each input channel relative to the start of each composite frame. The demultiplexing process may then use the captured phase information to align the reconstruction of the constituent channels relative to a reproduced constant frame rate.

6.17.2 <u>Setup Block Format.</u> In addition to defining the organization of the frames containing the multiplexed data, the ARMOR format incorporates the definition of a "setup block" that contains the parameters necessary to demultiplex the associated data frames. The setup block is included in the composite stream at the start of each recording to preserve with the data the information necessary to decode the data. Appendix L defines the setup block format and content.

6.17.3 <u>Multiplexer Format.</u> The definition of the ARMOR multiplex format has two parts. The frame structure definition describes the organization of the composite data frame which changes from one multiplex to the next. The channel coding definition describes the encoded data word format for each data type, which is the same for all multiplexers.

	Ste	p 1		2 3		4			5	6			7					
1	2	3	4					1	2		m	_		1	2		m	
	Sy	'nc		Fil (or tin code)	ler ne	PCM Channel Blocks		Fill	ler	PA Bl	PAR Channel Blocks			Filler				

Figure 6-17. The steps of the build process.

6.17.3.1 <u>Frame Structure.</u> The sequence of steps used to establish the multiplexed frame structure, shown in Figure 6-17, is explained in Table 6-18 below. The process involves putting the sync, PCM, parallel (PAR), time code, and analog channels into a frame. The filler blocks may consist of either constant (hex FF) bytes or analog samples, depending upon the constituent input channel mix. The PCM Sample Start Bit Point and the Parallel Sample Start Bit Point are based on calculations of the master oscillator, pacer, and the bit rate of the slowest PCM and word rate of the slowest parallel channels respectively. The pacer is a clock pulse that is programmed to a multiple of the fastest analog channel or the first word of the slowest parallel channel are not placed too early in the composite frame. If necessary to satisfy these Start Bit Point calculations, filler in the form of analog channel words or hex FF, if no analog words are available, is used to force the first PCM or PAR word later in the composite frame. Compatibility with specific legacy versions of the format requires the use of the appropriate equations, which are embodied in a software program, refer to Calculex Part No. 199034-0002².

²Part Number 199034-0002, available from CALCULEX, Inc., P.O. Box 339, Las Cruces, NM 88004 or by email to info@calculex.com.

TABLE 6-12. SCANLIST BUILD STEPS					
		(Reference scanlist in Figure 6-17)			
Step #1	Sync	The Sync is made up of four bytes of 8 bits totaling 32 bits: FE 6B 28 40			
Step #2	Time Code	If time code exists, it is placed after the sync in three words of bit length 24, 24, and 16. Multiple time codes are placed in ascending hardware sequence, as identified in the setup block.			
Step #3	Filler (PCM Start Bit)	If required, either filler or analog channels are placed next, depending on the calculation of the PCM Sample Start Bit Point. If no analog (or voice) channels are included in the multiplex, hex value "FF" filler is inserted in the frame as required to satisfy the PCM Sample Start Bit Point calculation. When analog channels are part of the multiplex, analog words are used in place of hex FF filler to minimize the formatting overhead.			
Step #4	PCM Channels	The PCM channels are placed next in ascending order of speed with the slowest channel first. Multiple channels at the same speed are placed in ascending hardware sequence, as identified in the setup block.			
Step #5	Filler (PAR Start Bit)	If required, either filler or analog channels are placed next, depending on the calculation of the PAR Sample Start Bit Point. If no analog (or voice) channels are included in the multiplex, hex FF filler is inserted in the frame as required to satisfy the PAR Sample Start Bit Point calculation. When analog channels are part of the multiplex, any remaining analog words that were not inserted in the frame at step 3 are used in place of hex FF filler to minimize the formatting overhead channel.			
Step #6	PAR Channels	The PAR channels are placed next in ascending order of speed with the slowest channel first. Multiple channels at the same speed are placed in ascending hardware sequence, as identified in the setup block.			
Step #7	Filler (Analog Channels)	All remaining analog words which have not been used for filler in steps 3 and 5 are placed next, followed by any additional filler required to satisfy the pacer divisor calculation.			

6.17.3.2 <u>Pacer Divisor Calculation</u>. The number of analog samples per ARMOR frame for each analog channel must be evenly divisible into the number of bits per ARMOR frame. The initial bits per ARMOR frame are calculated to minimize the aggregate bit rate of the composite.

Filler is then added to satisfy the divisibility rule to set the pacer clock speed. This step is referred to as the pacer divisor calculation, since the pacer itself is derived from the same master oscillator as the aggregate bit rate clock.

6.17.3.3 <u>ARMOR Channel Coding.</u> Each input data channel is encoded into 8-, 12-, 16-, or 24-bit words, depending on the type of channel. The bit length of an ARMOR frame is always an integer multiple of eight, so 12-bit words must occur an even (multiple of two) number of times within each frame. The data within a frame is serially concatenated most significant bit first. Table 6-19, which is an example of an ARMOR frame with two analog, one parallel, four PCM, and one time code channel, is referenced in the following descriptions.

TABLE 6-13. SAMPLE ARMOR FRAME					
Frame Item	Description	Words/Frame	Bits/Word		
Sync Pattern	X'FE6B2840'	1	32		
Time Code Ch #1	Encoded Time	2	24		
Time Code Ch #1	Encoded Time	1	16		
Filler	X'FF'	7	8		
PCM Ch #1	Encoded User Data	130	16		
PCM Ch #2	Encoded User Data	162	16		
PCM Ch #3	Encoded User Data	226	16		
PCM Ch #4	Encoded User Data	321	16		
Analog Ch #1	Encoded User Data	100	12		
Analog Ch #2	Encoded User Data	20	12		
Parallel Ch #1	Encoded User Data	2	16		
Parallel Ch #1	Encoded User Data	260	8		

6.17.3.4 <u>Sync Pattern</u>. All ARMOR frames begin with the fixed 32-bit sync pattern hexadecimal FE6B2840.

6.17.3.5 <u>Time Code Channels.</u> When time code channels are present in an ARMOR multiplex, their data words always immediately follow the sync pattern or another time code channel. Time is encoded as 64 bits in two 24-bit words and one 16-bit word. Table 6-20 defines the individual bits of the time code words. The encoded time is the time at the start of the ARMOR frame.

D	Day Of Year
Н	Hour of Day
Μ	Minutes past the Hour
S	Seconds past the Minute
MS	Milliseconds past the Second
HN	Hundreds of Nanoseconds past the Millisecond
SE	Sync Error (Time code decoding error)

NT	No Time Code (input signal detect fail)
0	Always Zero

<u>TABLE 6-14.</u>						
TIME CODE WORD FORMAT						
BIT WORD1 WORD2 WORD3						
23	D9	0				
22	D8	S 6				
21	D7	S5				
20	D6	S4				
19	D5	S 3				
18	D4	S2				
17	D3	S1				
16	D2	S 0				
15	D1	SE	0			
14	D0	NT	0			
13	0	0	HN13			
12	H5	0	HN12			
11	H4	MS11	HN11			
10	H3	MS10	HN10			
9	H2	MS9	HN9			
8	H1	MS8	HN8			
7	HO	MS7	HN7			
6	M6	MS6	HN6			
5	M5	MS5	HN5			
4	M4	MS4	HN4			
3	M3	MS3	HN3			
2	M2	MS2	HN2			
1	M1	MS1	HN1			
0	M0	MS0	HN0			

6.17.3.6 <u>PCM Channels.</u> User PCM data is encoded into 16-bit words. The number of 16-bit words (per channel) in each frame is approximately two percent greater than the number required to store the user data during the frame time period. These overhead words are included to compensate for minor variations in user data clock rates. In order to record the number of allocated frame bits which actually contain user data, the first two 16-bit words are redundant copies of a bit count. In Figure 6-19, PCM Channel #1 has 130 words: two count words and 128 data words. The bit count in either one of the redundant count words records the number of bits in the 128 data words that are actually

user PCM data (most significant bit first). All remaining bits are filler. The first user data bit in the most significant bit location of the third channel word (the first data word following the redundant count words) was the first bit to be received after the start of qqthe ARMOR frame.

6.17.3.7 <u>Analog Channels.</u> Analog data is digitized into either 8-bit or 12-bit samples using offset binary notation (a sample of X'00' or X'000' is the largest negative value). No overhead words or bits are included with analog channel data because input sampling is synchronous to the start of the ARMOR frame. The first sample of each channel was captured at frame start time with all remaining samples evenly spaced throughout the frame time. Note that the location of the analog channel words within the composite ARMOR frame has no correlation with the time between the start and end of the frame when the analog samples were captured (digitized). The first sample of the 100 Analog Channel #1 words and the first sample of the 20 Analog Channel #2 words in Figure 6-19 were both captured (digitized) at the same instant in time, which was the frame start time. Voice is a special case of an analog channel in that it is always 8-bit samples.

6.17.3.8 <u>Parallel Channels.</u> The encoding of parallel input channels is very similar to PCM encoding. Approximately two percent more than the minimum number of words necessary to store the user data during one ARMOR frame period are allocated to each parallel channel. The first two 16-bit words of each channel are redundant count words that record the actual number of allocated data words that contain user data. The remaining allocated words contain filler. Figure 6-19 has two entries for Parallel Channel #1. The first entry shows the two (redundant) 16-bit count words and the second entry shows the number of allocated 8-bit data words for the channel. The number of 8-bit data words that contain user data is determined by examining either of the two count words. The first data word for each parallel channel was the first word received after the start of the ARMOR frame.

6.17.4 <u>ARMOR Format Compatibility.</u> Compatibility with the ARMOR format can be divided into two distinct cases. In the first case, the user is playing back a legacy tape (made with legacy multiplexer hardware and software) on non-legacy demultiplexer hardware and software. In the second case, the user is creating a tape on non-legacy multiplexer hardware and software for future playback by legacy demultiplexer hardware and software.

In the first case, the legacy tape contains a setup block (see Section 6.17.2 above) at the start of the recording. The setup block contains the information necessary for the user to demultiplex the data records on the tape. The bit rate field in the setup block header section specifies the rate at which the legacy recording was generated. The saved scanlist field in the setup block trailer section specifies the exact sequence and size of the sync, data, and filler words in the recording.

In the second case, the user must first generate an ARMOR setup block at the start of the recording. Subsequent data records must then be formatted in accordance with the specification in the setup block. Setup Block creation is described in appendix L.

6.17.5 <u>ARMOR Format Validation</u>. The CALCULEX, Inc. ARMOR Format Verification Program (AFVP) may be used to determine if an independently generated multiplex is compatible with existing legacy hardware. The AFVP reads the setup block (see Section 6.17.2. above) from the data set under test and validates the data set frame structure. Please refer to IRIG 118, Vol III. The AFVP may be obtained from CALCULEX.³

³ Part Number 198007-0001 may be obtained from CALCULEX, Inc. P.O. Box 339, Las Cruces, NM 88004 or by email request to info@calculex.com.