APPENDIX G

ADARIO DATA BLOCK FIELD DEFINITIONS

LIST OF FIGURES

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APPENDIX G

ADARIO DATA BLOCK FIELD DEFINITIONS

1.0   Data Block Format and Timing

The details of the ADARIO data block format are provided in Figure G-1 and in the ADARIO data format field summary. As shown in Figure G-1, the eight session header words are the first eight words of the block. The channel packet for the highest priority (priority 1) channel is next, followed by the next lower priority channel packet (priority 2). Following the lowest priority channel, fill data consisting of all ones are inserted as required to complete the 2048-word data block.

Within the channel packet, the first five words are the channel header words including the partial word (PW). Following the channel header is the variable size channel data field. The channel data are organized in a last-in-first-out (LIFO) fashion. The first samples acquired in the block time interval appear in the last data word of the channel packet. The sample data are formatted into the 24-bit data word such that the first sample occupies the MSBs of the word. The next sample is formatted into the next available MSBs and so on until the word is full. As an example, data formatted into 8-bit samples is shown in Figure G-2.

In cases where the 24-bit data word is not a multiple of the sample size, the sample boundaries do not align with the data words. In these cases, the samples at the word boundaries are divided into two words. The MSBs of the sample appear in LSBs of the first buffered word and the LSBs of the sample appear in the MSBs of the next buffered word. Since the channel data appears in a LIFO fashion in the ADARIO data block, the MSBs of the divided sample will occur in the data word following the word containing LSBs of the sample. Figure G-3 depicts ADARIO timings.

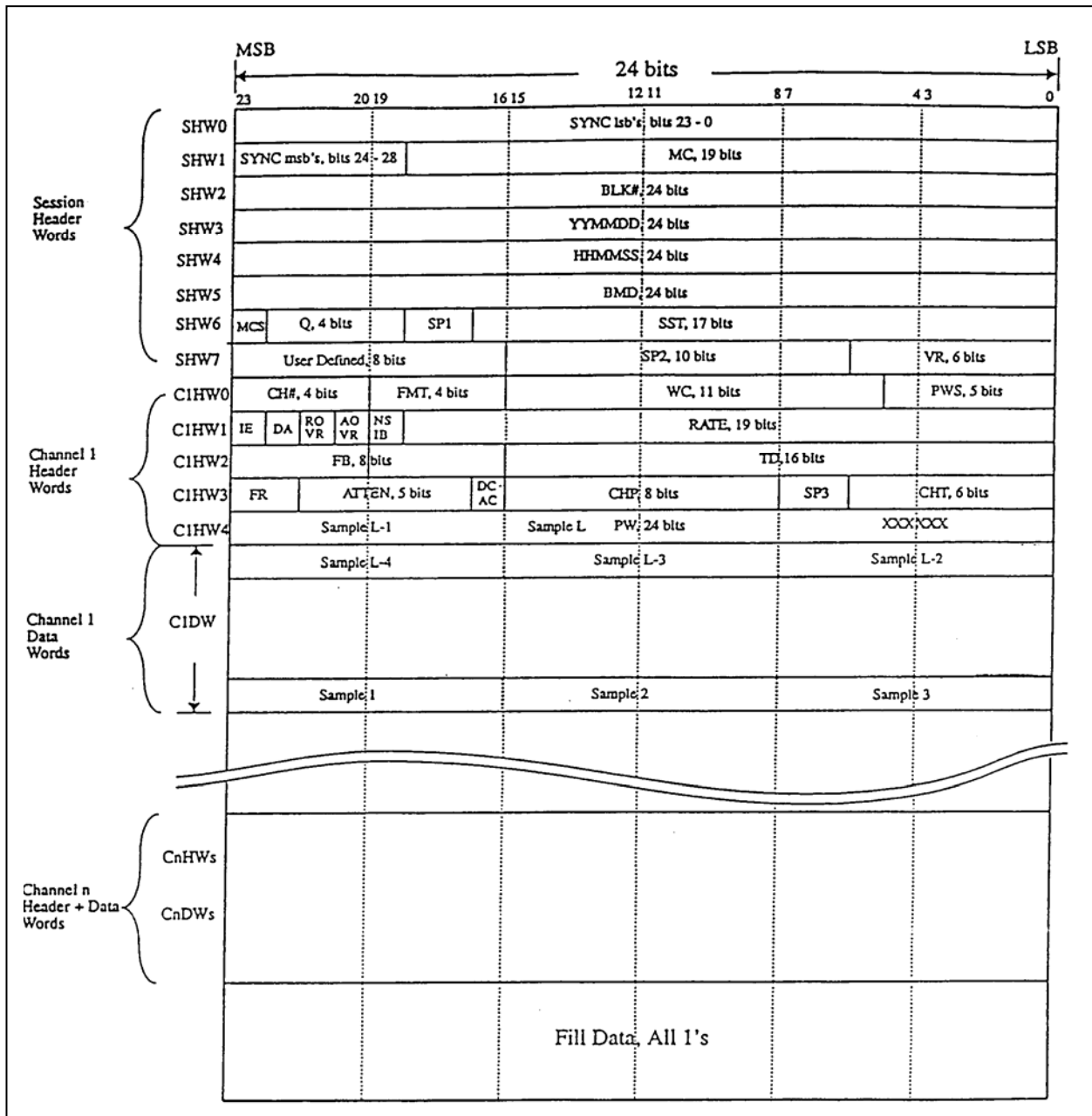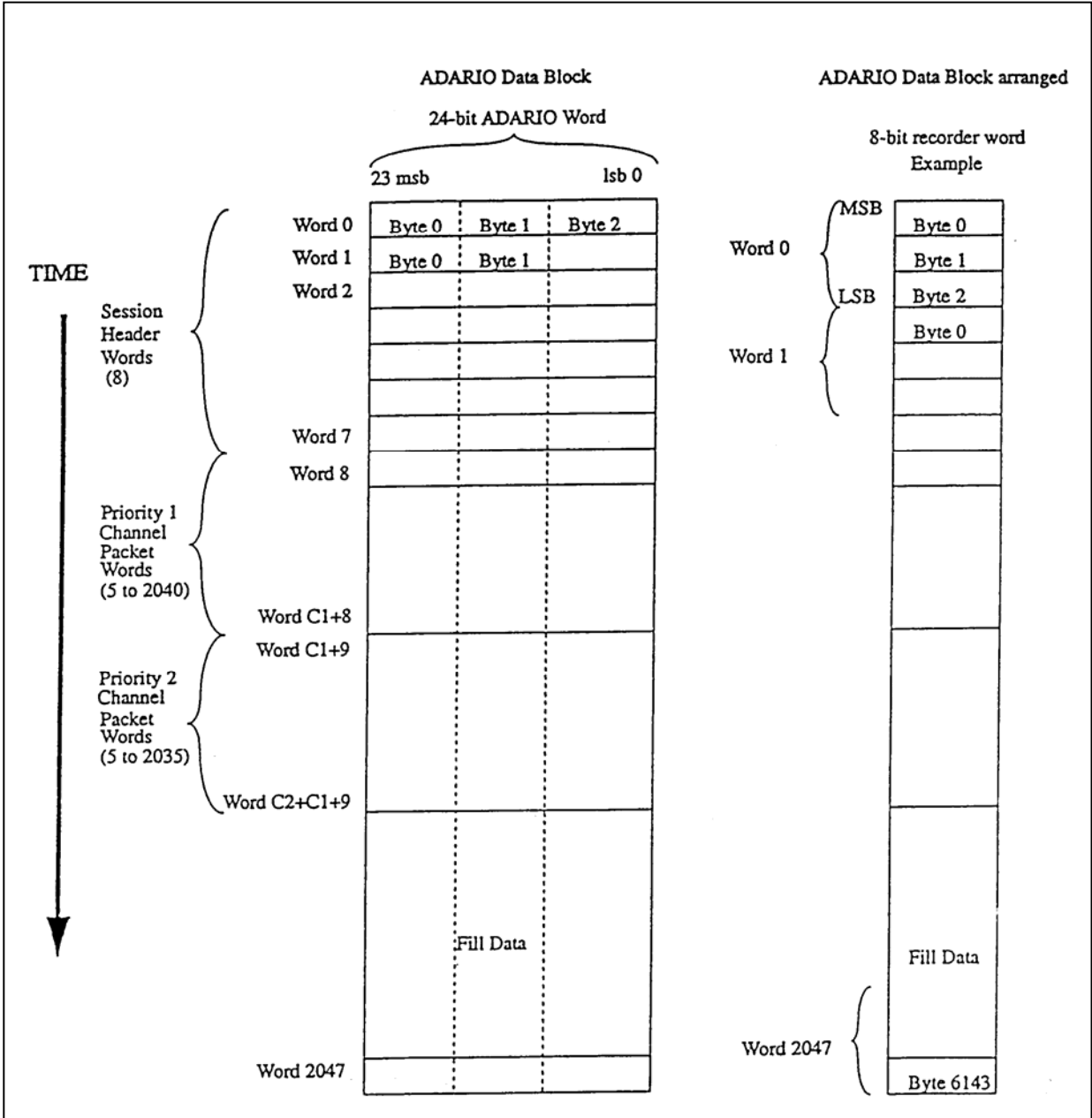Figure G-1.   ADARIO data format.

Figure G-2.   ADARIO data blocks.
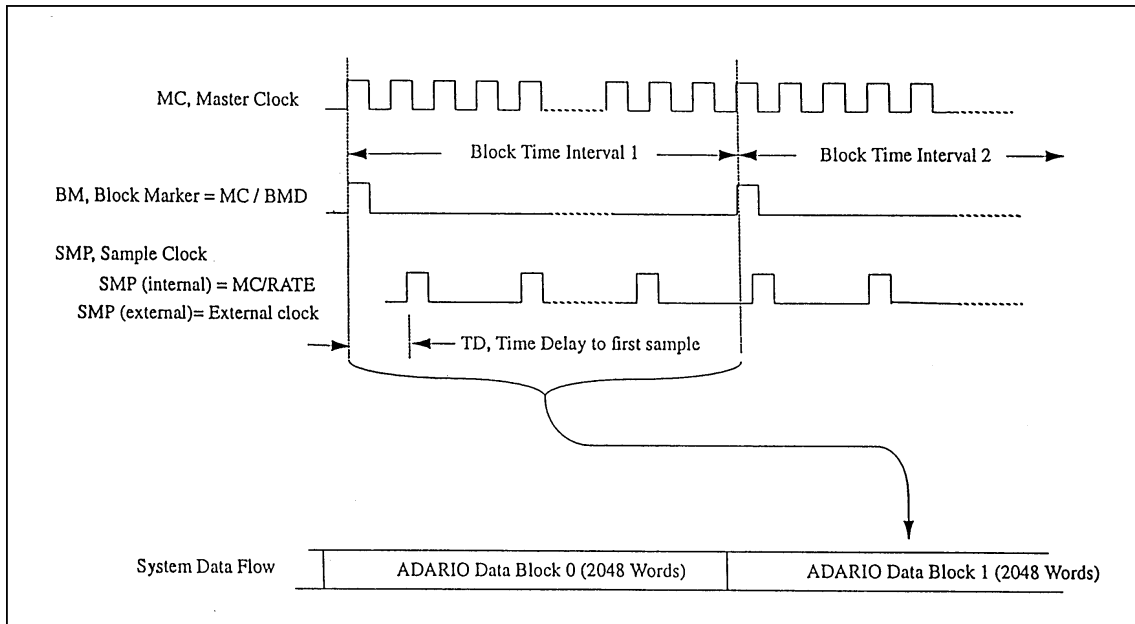
Figure G-3.   ADARIO timing.

2.0   **ADARIO Data Format Field Definitions Summary**

2.1   Block Length - (2048 words, 24-bit words, fixed length)

2.2   Session Header - (8 words, fixed format)

SHW0   (bits 23 to 0)   SYNC Field, bits 0-23 of the 29-bit block sync. The LSBs of the block sync are 36E19C and are contained here.

SHW1   (bits 23 to 19)   SYNC Field, bits 24-28 of the 29-bit block sync. The MSBs of the block sync are 01001 and are contained here. The 29-bit block sync is fixed for all ADARIO configurations and chosen for minimal data cross correlation.

           (bits 18 to 0)   MC, Master Clock, a 19-bit binary value in units of 250 Hz. MC is the clock frequency used to derive session and per channel parameters.

SHW2   (bits 23 to 0)   BLK#, ADARIO Data Block Number, a 24-bit binary value. BLK# is to zero at the start of each session and counts up consecutively. Rollover is allowed.

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SHW3 (bits 23 to 0) YYMMDD, Time Code Field, a BCD representation of the year (YY), month (MM), and day (DD). YYMMDD Time Code Field is updated during the record process once per second.

SHW4 (bits 23 to 0) HHMMSS, Time Code Field, a BCD representation of the hour (HH), minute (MM), and second (SS). The HHMMSS Time Code Field is updated during the record process once per second.

SHW5 (bits 23 to 0) BMD, Block Marker Divisor, a 24-bit binary value. BMD is established so that the block marker frequency, BM, may be derived from MC by $BM = MC/BMD$

SHW6 (bit 23) MCS, Master Clock Source, a 1-bit flag.
        1 = MC was generated internally.
        0 = MC was provided from an external source.

      (bits 22 to 19) Q, Number of active channels minus one, a 4-bit binary value. For example, 0 indicates that one channel is active.

      (bits 17 to 18) SP1, Spare field 1, a 2-bit field. It is set to zero.

      (bits 16 to 0) SST, Session Start Time, a 17-bit binary value in units of seconds. The integer number of seconds represents the session start time of day in seconds, where midnight starts with zero.

SHW7 (bits 23 to 16) User Defined, an 8-bit field. May be input by the user at any time during a recording session. The interpretation of this bit field is left to the user.

      (bits 15 to 6) SP2, Spare field 2, a 10-bit field. It is set to zero.

      (bits 5 to 0) VR, Version number, a 6-bit binary value. Each update of the ADARIO format will be identified by a unique version number.

2.3 Channel 'n' Header — All channel headers contain five 24-bit ADARIO words with the following fixed format. The first logical channel, n=1, has the highest priority and its channel packet starts in the ninth word of the data block. Each active channel is represented by a channel packet that is present in the data block. The logical channel number, n, represents the relative priority of the channel and the order in which it appears in the data block.

CnHW0   (bits 23 to 20)   CH#, Physical Channel Number, a 4-bit binary value. 0 to 15 represents the physical location of the channel electronics in the ADARIO hardware. The user sees those locations labeled from 1 to 16.

(bits 19 to 16)   FMT, Format code for the channel data word, a 4-bit binary value. The format code is used to define the size of the user data word by means of the following table:

15 = 24 bits	7 = 8 bits
14 = 22 bits	6 = 7 bits
13 = 20 bits	5 = 6 bits
12 = 18 bits	4 = 5 bits
11 = 16 bits	3 = 4 bits
10 = 14 bits	2 = 3 bits
9 = 12 bits	1 = 2 bits
8 = 10 bits	0 = 1 bit

(bits 15 to 5)   WC, Word Count, an 11-bit binary value. WC is the number of full channel data words that should be in the nth channel packet. WC may range from 0 to 2040. A WC greater than the number of actual words in channel packet indicates a data rate overflow, which would occur when a low-priority channel is not provided sufficient space in the fixed length data block as a result of an uncontrolled data rate in a higher priority channel.

(bits 4 to 0)   PWS, Partial Word Status, a 5-bit binary value. PWS is related to the number of samples in the partial word and may range from 0 to 23. PWS shall be computed as follows:

   If the number of full samples in the partial word equals zero, then PWS = 0.

   If the number of full samples in the partial word does not equal zero, then PWS = Round Up [Unused bits In PW/Channel Sample Size].

CnHW1 (bit 23)   IE, Channel Clock Source, a 1-bit flag.
                             1 = The channel clock was generated internally.
                             0 = The channel clock was provided from an external
                             source.

        (bit 22)   DA, Data type, a 1-bit flag.
                             1 = The channel is operated as a digital channel.
                             0 = The channel is operated as an analog channel.

        (bit 21)   ROVR, Rate overrun in previous block, a 1-bit flag.
                             1 = The nth channel packet in the previous data block
                             experienced an overrun.
                             0 = The nth channel packet in the previous data block
                             did not experience an overrun.

        (bit 20)   AOVR, Analog A/D Overrange in current block a 1-bit
                          flag.
                             1 = The nth channel in the current data block
                             experienced an analog-to-digital conversion overrange
                             condition.
                             0 = The nth channel in the current data block did not
                             experience an analog-to-digital conversion overrange
                             condition.

        (bit 19)   NSIB, No samples in current block, a 1-bit flag.
                             1 = TRUE, there are no samples for the nth channel in
                             the current block.
                             0 = False, there are samples for the nth channel in the
                             current block.

        (bits 18 to 0)   RATE, Channel sample rate indicator, 19-bit binary value.
                          The interpretation of the rate value depends on the
                          condition of IE, the channel clock source flag.
                                 If IE = 1, then the value of rate is carried by the 16
                          LSBs of the rate field. Using rate, the frequency of the
                          internal channel clock can be found by internal sample
                          clock = (MC/RATE) -1.
                                 IF IE = 0, then rate is a 19-bit binary value in units of
                          250 Hz which equals the frequency of the external channel
                          clock as provided by the user at the time of the setup.

* **CnWD2** (bits 23 to 16)   FB, Filter Bandwidth, an 8-bit binary value. The formula for the bandwidth, BW, of the anti-aliasing filter used in an analog channel incorporates FB as $BW = (FB/2) \bullet 10^{3+FR}$

                   (bits 15 to 0)   TD, Time Delay to first sample, a 16-bit binary value. TD is a measure of the time delay from the block marker, BM, to the first sample arriving at the nth channel during the current data block interval. TD is expressed as the number of master clock, MC, periods minus one.

* **CnWD3** (bits 23 to 22)   FR, Filter Range, a 2-bit binary value. The formula for the bandwidth, BW, of the anti-aliasing filter used in an analog channel corporates FR as $BW = (FB/2) \bullet 10^{3+FR}$

                   (bits 21 to 17)   ATTEN, Attenuation, a 5-bit binary value. ATTEN represents the setting of the input attenuator (or gain) on the nth channel at the time that the record was formed $0 = -15dB$ and $31 = +16dB$ with intermediate settings expressed in one dB steps.

                   (bit 16)   DCAC, Analog signal coupling, a 1-bit flag.
                                 1 = The channel is operated with dc coupling at the input.
                                 0 = The channel is operated with ac coupling at the input.

                   (bits 15 to 8)   CHP, Channel Parameter field, an 8-bit field. The interpretation of the CHP field depends upon the card type with which it is associated, as defined by the CHT field. Each card type established by the CHT field, as part of its definition, shall specify the form and interpretation of the CHP field. To date, four input card types have been established. The CHP fields are defined as follows:

            *   For CHT=0

(bits 15 to 8)   remain undefined for the present analog single channel implementation except that the present hardware implementation expects an all zero field. Would be subject to future definition as long as all the zero fill is set aside.

            *   For CHT=1

(bits 15 to 8)   remain unused for the present digital single channel implementations except that the present hardware implementation expects an all zero field. Would be subject to future definition as long as the all zero fill is set aside.

            *   For CHT=2

(bits 15 to 8)   remain unused for the present dual-purpose channel implementations except that the present hardware implementation expects an all zero field. Would be subject to future definition as long as the all zero fill is set aside.

                      For CHT=3

(bits 15 to 12)   establish the number of subchannels that are multiplexed into the multichannel data carried by the nth channel.

(bits 11 to 8)   identify the subchannel number of the first sample contained in the nth channel packet of the data block.

(bits 7 to 6)   SP3, Spare field 3, a 2-bit field. It is set to zero.

(bits 5 to 0)   CHT, Channel Type, a 6-bit field. Defines the type of channel through which input data was acquired. Additional channel types to be defined by future users and developers.

        *   CHT=0 Single channel analog input
        *   CHT=1 Single channel digital input
        *   CHT=2 Single channel, dual-purpose, analog or digital input
        *   CHT=3 Multichannel analog input capable of multiplexing
                up to 16 analog inputs
        *   CHT=4 Single channel digital input, dual channel analog
                    input (stereo)
                    "L" channel on bits 15 to 8 of the sample word,
                    "R" channel on bits 7 to 0 of the sample word
           CHT=5 Single channel, triple-purpose, analog, digital, submux, formatted input

CnWD4   (bits 23 to 0)   PW, Partial Word, A 24-bit field. PW contains the last samples of the data block. The most significant bits of

word contain the first sample, followed by the next sample in the next most significant bits. The number of samples in the PW is defined in the PWS field. The unused bits are not intentionally set and so contain random data.

Fill   (bits 23 to 0)   Fill, Fill Words consisting of all ones binary, used for fixed rate aggregate. Fill words may be omitted when variable rate aggregate can be accommodated resulting in variable length blocks of up to 2048, 24-bit words.

3.0   Submux Data Format Field Definitions

The details of the submux data format are shown in Figures G-4a and b and defined in the Submux Data Format Field Definitions Summary. Figure G-5 shows a typical primary channel aggregate data content for fixed and variable rate channel. Submux data format is based on the sequential collection of the individual channel data blocks. Each channel data block is the sequential collection of presented input samples in a fixed period of time. This sequential collection results in a variable length, fixed rate, and channel data blocks. To accommodate fixed rate channels, fill is also defined. The aggregate data stream is composed of a block sync timing channel, followed by sequential channel data blocks, if enabled, followed by fill, if required, at fixed block rate.

The channel data blocks are the sequential collection of input samples bit packed into sequential 16-bit words over the block period of time. The data block is preceded by a three-word header that identifies the source (channel ID) of data, channel type of processing, packing format in the data block, bit count length of the valid data, and the time delay between the first sample and the block period. If data were internally sampled, the sample period is defined with the first sample being coincident with the start of block period. Channel type is used to define specific types of channels that provide timing, annotation, and synchronization functions that may be required by the specific primary channel or may be redundant and not required. Specific implementation of the required channels may provide only the required channels with specific implementation constraints that limit the aggregate rate or the range of any specific field.

The submux format is based on a 16-MHz clock defining all timing. The derived clock is the 16-MHz clock divided in binary steps as defined by 2^{BRC} that defines all timing and internal sampling. Block period is 20 160 derived clock periods which limits the submux aggregate to 256 Mbps, limits the maximum block rate to 793.65 blocks per second, and in conjunction with a 16-bit bit count field, limits the subchannel maximum data rate to 52 Mbps.

4.0   SubMux Data Format Field Definitions Summary

4.1   <u>Frame length</u>. Variable or fixed with fill. Minimum is 3-word block sync plus one
        channel block, maximum is 20 160x16-bit words.

4.2   <u>Block length</u>: Variable from 3x16-bit words to 4099x16-bit words per channel data
        block. Specified by CHT>0 and integer of (Bit_Count+15/16). May be
        limited by implementation.

4.3   <u>Block sync</u>: Defined by Channel ID = 31, 3-word block, 2-word sync. Defines a
        period of 20 160 derived clocks.

4.4   <u>General form</u>: All Channel data blocks contain this information in the 3-word header.

        HW1   (bits 15 to 11)   CHN ID, Channel ID number, from 0 to 30 binary number
                                represents normal channel of any type. CHN ID = 31 reserved for
                                Block Sync.

               (bits 10 to 8)   CHT, Channel Type, from 0 to 7 defines type of processing
                                performed on the data and the format of header word fields.

                                CHT = 0   Timing channel, block sync or time tag, 3-word
                                             only
                                CHT = 1   Annotation text or block count, variable length
                                CHT = 2   Digital serial external or internal clock, variable
                                CHT = 3   Digital parallel external clock, variable
                                CHT = 4   Analog wide band, variable
                                CHT = 5   Analog stereo, variable
                                CHT = 6   TBD (to be defined by future implementation)
                                CHT = 7   TBD

        <u>Variable length</u>:   General form with variable data block length

        HW1   (bits 15 to 11)   CHN ID, Channel ID number, from 0 to 30 binary number
                                represents normal channel of any type.

               (bits 10 to 8)   CHT, Channel Type, from 1 to 7 defines type of processing
                                performed on the data and the format of header word fields.

               (bits 7 to 4)   FMT, Format, defines the number of bits minus one in each
                                sample. Data block sample size (bits) = (FMT+1). Range 0 to
                                15, binary format.

               (bits 3 to 0)   ST1 to ST4, status bits, define dynamic conditions within this
                                block period such as over range.

HW2 (bits 15 to 0)   Bit_Count defines the number of valid data bits in the data block starting with the most significant bit of the first data word DW1. Variable word length of the data block is the Integer of $\{(Bit\_Count + 15)/16\}$. Range 0 to 65 535, binary format.

HW3 (bit 15)   I/E, Internal/External clock

    (bits 15 to 0)   Depends on CHT field, defines block count, time delay, or sample period.

4.5   Block Sync: Defines the start of channel data blocks and start of block period that lasts for 20 160 derived clocks.

HW1 (bits 15 to 0)   SYNC 1 = F8C7 hex, defines the first sync word.

HW2 (bits 15 to 0)   SYNC 2 = BF1E hex, defines the second sync word.

HW3 (bits 15 to 13)   BRC, Block Rate Clock, defines the binary divisor for the 16 MHz system clock. Derived CLK = 16 MHz / 2^{BRC} MHz. Block rate = Derived CLK / 20 160 Hz.   Period = 1 / Derived CLK.

    (bit 12)   FILL, indicates if the primary channel requires fill for constant rate.

    (bits 11 to 4)   TBD

    (bit 3)   AOE, Aggregate Overrun Error if set indicates that the aggregate of the enabled channels exceeds the submux aggregate (data truncated to 20 160 words between sync).

    (bit 2)   PCRE, Primary Channel Rate Error if set indicates that primary channel is unable to maintain the aggregate rate of the submux. Excess blocks are truncated.

    (bits 1 to 0)   ST3, ST4, Status reserved.

4.6   Time Tag: Defines the time tag channel for time stamping the frame.

HW1 (bits 15 to 11)   CHN ID, Channel ID number, from 0 to 30 binary number represents normal channel.

    (bits 10 to 8)   CHT = 0, Channel Type = 0, Time Tag IRIG Time code processing and 3-word format.

HW   (bits 7 to 0)   DAYS, Most significant 8 bits of Time Code Days field. BCD format.

	(bits 15 to 14)	DAYS, Least significant 2 bits of Time Code Days field. BCD format.
	(bits 13 to 8)	HOURS, Time Code Hours 6 bit field. BCD format.
HW	(bits 7 to 0)	MINUTES, Time Code Minutes 7 bit field. BCD format.
	(bits 15 to 8)	SECONDS, Time Code Seconds 7 bit field. BCD format.
	(bits 7 to 0)	FRACTIONAL SECONDS, Time Code Fractional Seconds 8 bit field. BCD format.

4.7   <u>Annotation Text:</u>   Defines block count and annotation text that pertains to the subchannels at this time.

HW1	(bits 15 to 11)	CHN ID, Channel ID number, from 0 to 30 binary number represents normal channel.
	(bits 10 to 8)	CHT = 1, Channel Type = 1, Block Count and Annotation Text if any.
	(bits 7 to 4)	FMT = 7, Format = 7, defines 8 bit ASCII character in text.
	(bit 3)	NC, No Characters (Bit_Count = 0) Block count only.
	(bits 2 to 0)	OVR, PE, OE, Overrun Parity and async framing error.
HW	(bits 15 to 0)	Bit_Count defines the number of valid data bits in the data block starting with the MSB of the first data word DW1. Variable word length of the data block is the Integer of {(Bit_Count + 15)/16}. Range 0 to 65 535, binary format.
HW	(bits 15 to 0)	Block_Count sequential block numbering with rollover at maximum. Range 0 to 65 535, binary format.
DW1	(bits 15 to 8)	1st CHARACTER, first text character.
DW	(bits 8 or 0)	Last CHARACTER, LSB is defined by the Bit Count.

4.8   <u>Digital Serial External CLK</u>: Defines digital serial data such as PCM externally clocked.

| HW1 | (bits 15 to 11) | CHN ID, Channel ID number, from 0 to 30 binary number represents normal channel. |

(bits 10 to 8)   CHT = 2, Channel Type = 2, digital serial or data and clock over sampled data.

(bits 7 to 4)   FMT = 0 Format = 0, defines 1-bit data samples.

(bit 3)   NSIB, No Samples In Block (Bit_Count=0) header only.
(bit 2)   OVR, Overrun indicates that input is clocking at faster than specified rate. Data is truncated at specified bit rate (Bit Count per Block).

HW   (bits 15 to 0)   Bit_Count, defines the number of valid data bits in the data block starting with the most significant bit of the first data word DW1. Variable word length of the data block is the Integer of $\{(\text{Bit\_Count} + 15)/16\}$. Range 0 to 65 535, binary format. Limited by set maximum rate.

HW   (bit 15)   I/E = 0, Internal / External clock flag indicates that external clocking was used with relative phasing to block as specified in next field.

(bits 14 to 0)   Time Delay provides the measure of time between start of block period and the first external clock in derived clock periods. Range 0 to 20 160, binary format.

DW1   (bit 15) DS_1, first data sample at the first clock time in the block.

Dw_n (bit L) DS_L, last data sample in this block period.

4.9 Digital Serial Internal CLK: Defines digital serial data low rate (> 2 samples per block period) internally oversampled.

HW1   (bits 15 to 11)   CHN ID, Channel ID number, from 0 to 30 binary number represents normal channel.

(bits 10 to 8)   CHT = 2, Channel Type = 2, Digital serial or data and clock over sampled data.

(bits 7 to 4)   FMT = 0 Format = 0, defines 1-bits data samples.
(bits 3 to 0)   0, reserved.

HW2   (bits 15 to 0)   Bit_Count defines the number of valid data bits in the data block starting with the most significant bit of the first data word DW1. Variable word length of the data block is the Integer of $\{(\text{Bit\_Count} + 15)/16\}$. Range 0 to 65 535, binary format. Limited by set maximum rate.

HW3   (bit 15)   I/E = 1, Internal Sampling flag indicates that internal sampling was used as specified in next field.

      (bits 14 to 9)   TBD

      (bits 8 to 0)   SAMPLE PERIOD, defines the period of the over-sampling clock that samples data and clock, in derived clock periods. Range 0 to 4 mega samples per second, binary format.

DW1   (bit 15) DS_1, first data sample at block time.

      (bit 7) CS_1, first clock sample at block time.

DWn   (bit 8) DS_L, last data sample in this block period.

      (bit 0) CS_L, last clock sample in this block period.

4.10   <u>Digital Parallel External CLK</u>: Defines digital data including serial externally clocked.

HW1   (bits 15 to 11) CHN ID, Channel ID number, from 0 to 30 binary number represents normal channel.

      (bits 10 to 8)   CHT = 3, Channel Type = 3, Digital parallel or serial data.

      (bits 7 to 4)   FMT, Format, defines the number of bits minus one in each sample. Data block sample size   (bits) = (FMT+1). Range 0 to 15, binary format.

      (bit 3)   NSIB, No Samples In Block (Bit_Count = 0) Header only.

      (bit 2)   OVR, Overrun indicates that input is clocking at faster than specified rate. Data is truncated at specified bit rate (Bit Count per Block).

HW2   (bits 15 to 0)   Bit_Count defines the number of valid data bits in the data block starting with the most significant bit of the first data word DW1. Variable word length of the data block is the Integer of ((Bit_Count + 15)/16). Range 0 to 65 535, binary format. Limited by set maximum rate.

HW3   (bit 15)   I/E = 0, Internal / External clock flag indicates that external clocking was used with relative phasing to block as specified in next field.

(bits 14 to 0)   Time delay provides the measure of time between start of block period and the first external clock in derived clock periods. Range 0 to 20 160, binary format.

DW1   (bit 15) DS_1, MSB of the first data sample at the first clock time in the block.

DW_n (bit L) DS_L, LSB of the last data sample in this block period.

4.11 Analog Wide Band: Defines analog wide band data using a sampling A/D and internal block synchronous clock.

HW1   (bits 15 to 11)   CHN ID, Channel ID number, from 0 to 30 binary number represents normal channel.

(bits 10 to 8)   CHT = 4, Channel Type = 4, analog wide band sampled data.

(bits 7 to 4)   FMT, Format, defines the number of bits minus one in each sample. Data block Sample Size   (bits) = (FMT+1). Range 0 to 15, binary format. Limited by the A/D resolution.

(bit 3)   AOR, Analog over range (A/D 4-msb = F).

(bits 2 to 0)   ST2 to ST4, reserved status

HW2   (bits 15 to 0)   Bit_Count defines the number of valid data bits in the data block starting with the MSB of the first data word DW1. Variable word length of the data block is the Integer of ((Bit_Count + 15)/16). Range 0 to 65 535, binary format. Limited by set maximum rate.

HW3   (bit 15)   I/E = 1, Internal Sampling flag indicates that internal sampling was used as specified in next field.

(bits 14 to 12)   TBD

(bits 11 to 0)   Sample Period defines the period of the over-sampling clock that samples data and clock, in derived clock periods. Range 0 to 4m samples per second, binary format.

DW1   (bit 15) DS_1, MSB of the first data sample at the first clock time in the block.

DW_n (bit L) DS_L, LSB of the last data sample in this block period.

4.12   Analog Stereo "L" & "R": Defines analog stereo data using a sigma-delta A/D and internal   block synchronous clock with tracking Finite Impulse Response (FIR) filter.

HW1 (bits 15 to 11)   CHN ID, Channel ID number, from 0 to 30 binary number represents normal channel.

(bits 10 to 8)   CHT = 5, Channel Type = 5, Analog stereo voice band data.

(bits 7 to 4)   FMT, Format defines the number of bits minus one in each sample. Data block sample size   (bits) = (FMT+1). Range 0 to 15, binary format. Limited by the A/D resolution.

(bit 3)   LAOR, left subchannel over range.

(bit 2)   RAOR, right subchannel over range.

(bits 1 to 0)   ST2 to ST4, reserved status.

HW2 (bits 15 to 0)   Bit_Count defines the number of valid data bits in the data block starting with the MSB of the first data word DW1. Variable word length of the data block is the Integer of {(Bit_Count + 15)/16}. Range 0 to 65 535, binary format. Limited by set maximum rate.

HW3 (bit 15)   I/E = 1, Internal Sampling flag indicates that internal sampling was used as specified in next field.

(bit 14)   ENL, Enable Left subchannel.

(bit 13)   ENR, Enable Right subchannel.

(bit 12)   TBD

(bits 11 to 0)   Sample period defines the period of the over-sampling clock that samples data and clock, in derived clock periods. Range 3.76 to 40K samples per second, binary format.

DW1 (bit 15) DS_1, MSB of the first data sample left subchannel if enabled.

(bit 15- (FMT-1) DS_1, MSB of the first data sample right subchannel if enabled, else second sample.

DWn (bit L) DS_L, LSB of the last data sample in this block period.

4.13   <u>Fill</u>: Defines fill word that can be inserted at the end of all channel data blocks if required by the constant rate primary channel.

Fwx   (bits 15 to 0)   FILL, defined as FFFF hex word.

Figure G-4a — Submux data format

16 BITS

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

General Form

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HW1	CHN ID						CHT			FMT			ST1	ST2	ST3	ST4
HW2																
HW3	I/E	TIME DELAY or SAMPLE PERIOD														

Frame Sync

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HW1	CHN ID = 1F						CHT = 0			SYNC 1 = F8C7 hex (full word)						
HW2	SYNC 2 = BF1E hex															
HW3	BRC			FILL									AOE	PCR	ST3	ST4

Time Tag

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HW1	CHN ID = 0 to 30						CHT = 0		MSB	DAYS (BCD)						
HW2	DAYS lsb		HOURS (BCD) lsb						MINUTES (BCD) lsb							
HW3	SECONDS (BCD) lsb								FRACTIONAL SECONDS lsb							

Annotation Text

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HW1	CHN ID = 0 to 30						CHT = 1			FMT = 7			NC	OVR	PE	OE
HW2	BIT_COUNT															
HW3	BLOCK COUNT															
DW1	msb 1ST CHARACTER lsb								msb 2ND CHARACTER 1sb							
:																
DWn	msb Last CHARACTER lsb								UNDEFINED if not last							

Digital Srl. Ext. CLK

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HW1	CHN ID = 0 to 30						CHT = 2		FMT = 0				NSIB	OVR	ST3	ST4
HW2	BIT_COUNT = L															
HW3	I/E=0	TIME DELAY														
DW1	DS1	DS2	DS3	DS4	DS5	DS6	DS7	DS8	DS9	DS1	DS1	DS1	DS1	DS1	DS1	DS1
:																
DWn							DS$_{L-1}$	DS$_L$	UNDEFINED if not last							

Figure G-4a.   Submux data format.

		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Digital Serial Int. CLK	HW1	CHN ID = 0 to 30							CHT = 2			FMT = 0			0	0	ST3	ST4
	HW2	BIT_COUNT = L															
	HW3	I/E=1							SAMPLE PERIOD								
	DW1	DS_1	DS_2	DS_3	DS_4	DS_5	DS_6	DS_7	DS_8	CS_1	CS_2	CS_3	CS_4	CS_5	CS_6	CS_7	CS_8
	:																
	DWn	DS_{L-7}	DS_{L-6}	DS_{L-5}	DS_{L-4}	DS_{L-3}	DS_{L-2}	DS_{L-1}	DS_L	CS_{L-7}	CS_{L-6}	CS_{L-5}	CS_{L-4}	CS_{L-3}	CS_{L-2}	CS_{L-1}	CS_L
Digital Parallel Ext. CLK	HW1	CHN ID = 0 to 30							CHT = 3			FMT=0 to 15 (shown =6)			NSIB	OVR	ST3	ST4
	HW2	BIT_COUNT = L															
	HW3	I/E=0							TIME DELAY								
	DW1	MSB	1ST SAMPLE						MSB	2ND SAMPLE						3RD SAMPLE	
	:																
	DWn			MSB Last SAMPLE LSB=bit L						UNDEFINED if not last							
Analog Wide Band	HW1	CHN ID = 0 to 30							CHT = 4			FMT=0 to 15 (shown =7)		AOR	ST2	ST3	ST
	HW2	BIT_COUNT = L															
	HW3	I/E=1				SAMPLE PERIOD											
	DW1	MSB	1ST SAMPLE						MSB	2nd SAMPLE							
	:																
	DWn	MSB	Last SAMPLE LSB=bit L						UNDEFINED if not last							
Analog Stereo "L" & "R"	HW1	CHN ID = 0 to 30							CHT = 5			FMT=0 to 15 (shown =7)		LAOR	RAOR	ST3	ST4
	HW2	BIT_COUNT = L															
	HW3	I/E=1	ENL	ENR		SAMPLE PERIOD											
	DW1	MSB	1ST SAMPLE "L"						MSB	1ST SAMPLE "R"							
	:																
	DWn	MSB	Last SAMPLE						UNDEFINED if not last							
Fill	FW	Fill Word = FFFF hex															

Figure G-4b.   Submux data format.

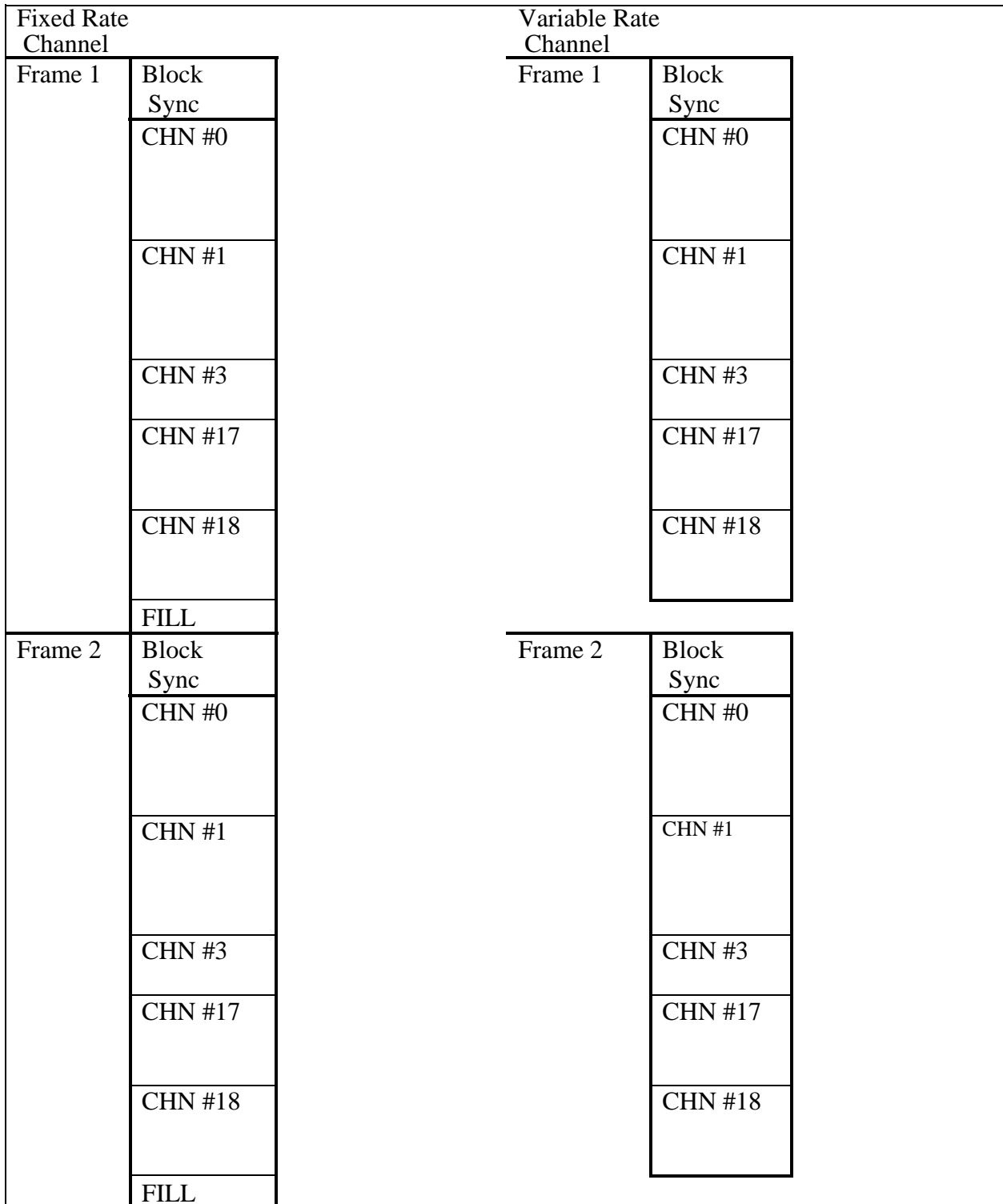| Fixed Rate Channel		Variable Rate Channel	
Frame 1	Block Sync	Frame 1	Block Sync
	CHN #0		CHN #0
	CHN #1		CHN #1
	CHN #3		CHN #3
	CHN #17		CHN #17
	CHN #18		CHN #18
	FILL		
Frame 2	Block Sync	Frame 2	Block Sync
	CHN #0		CHN #0
	CHN #1		CHN #1
	CHN #3		CHN #3
	CHN #17		CHN #17
	CHN #18		CHN #18
	FILL		

Figure G-5.   Submux aggregate format.

**** END OF APPENDIX G ****